Laboratory 5

(Due date: June 17th)

OBJECTIVES

- ✓ Learn the Partial Reconfiguration (PR) flow using the Vivado TCL console for embedded systems (PS+PL).
- ✓ Generate: i) full bitstreams, ii) partial bitstreams, and iii) blanking bitstreams.
- ✓ Perform partial reconfiguration on the ZYBO (or ZYBO Z7-10) Board via software using the PCAP interface.

VHDL CODING

- ✓ Refer to the Tutorial: VHDL for FPGAs for a tutorial and a list of examples.
- ✓ Refer to the Tutorial: Embedded System Design for Zynq PSoC for information on the Partial Reconfiguration Flow using the Vivado TCL console as well as examples.

FIRST ACTIVITY (100/100) – DYNAMIC PIXEL PROCESSOR

- Download the project files of the Dynamic Pixel Processor available in the Embedded System Design for Zynq PSoC Tutorial → Unit 7. The files are for the dynamic implementation of the Pixel Processor system.

- Follow the procedure detailed in the Tutorial – Unit 7, but generate 5 configurations:
  - ✓ `pixfull_rp`: Variant with F=1.
  - ✓ `pixfull_rp`: Variant with F=2.
  - ✓ `pixfull_rp`: Variant with F=3.
  - ✓ `pixfull_rp`: Variant with F=4.
  - ✓ `pixfull_rp`: Variant with F=5.

  Make sure to generate the correct `.bin` files to successfully program them via the PCAP (see Tutorial – Unit 7).

- Generate the 5 partial bitstreams, the 5 full bitstreams, along with the blanking bistream.
- Modify the SDK project `pixtst_rp` (in Tutorial – Unit 7) to:
  - ✓ Load the five partial bitstreams from the SD card.
  - ✓ Program each partial bitstream and get results from each case (using the same input provided in Tutorial – Unit 7).

PARTIAL RECONFIGURATION DEMO

- Download the full bitstream of the configuration with F=1. Program the device.
- Use the modified SDK project `pixtst_rp` to test the pixel processor. The expected results from applying the five partial bitstreams are indicated below. **Demonstrate this to your instructor**.

INPUT	OUTPUT				
	RP. F=1	RP. F=2	RP. F=3	RP. F=4	RP. F=5
0xDEADBEEF	0xEED2DDF7	0xC1758DDF	0x5D928242	0x051B1101	0xC0A5B0C7
0xBEBEDEAD	0xDDDDEED2	0x8D8DC175	0x82825D92	0x1111051B	0xB0B0C0A5
0xFADEBEAD	0xFDEEDDD2	0xF4C18D75	0x275D8292	0x0005111B	0xCBC0B0A5
0xCAFEBEDF	0xE3FFDDEF	0x9FFC8DC2	0x7617825C	0X0B001104	0xB7CCB0C1

- Submit (as a .zip file) the following to Moodle (an assignment will be created). DO NOT submit the whole PR project. You can work in groups of 2 and only have one submission.
  - ✓ The /Sources folder: This contains all the sources (.vhd, .xdc) files.
  - ✓ The /Bitstreams folder: This contains all the bitstreams you generated.
  - ✓ The design.tcl file.
  - ✓ The .c and .h files that make up your `pixtst_rp` SDK project.

Instructor signature: _____ **Date:** _____